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Proposed Interview Agenda

In Amendment C filed March 18, 2009, the Applicant presented the argument that the Kakizawa reference teaches only a single analog loop back path and thus does anticipate or render obvious that a plurality of switching transistors provide for a plurality of internal test signal paths between an input pad and an output pad of the high-speed data interface of an integrated circuit. In response to this argument, the Examiner asserted in the Office Action dated June 1, 2009, that Kakizawa does indeed disclose a plurality of switching transistors (190, 192, 290, 292) for providing a plurality of internal test signal paths. Specifically, the Examiner asserted that Kakizawa discloses two paths: one loop back path 199 controlled by transistors 190 and 192, and another loop back path 299 controlled by transistors 290 and 292. The Applicant believes that this view of the teachings of Kakizawa is incorrect and would like to discuss this point during the telephone interview.

It is the Applicant's position that although Kakizawa uses two separate reference numbers 199 and 299, only a single loop back path is present. This position is supported by multiple portions of the disclosure of Kakizawa. First, in paragraph [0015], Kakizawa teaches "transmitter pins 110 and 112 are each coupled to the corresponding receiver pins via the transistors 190 and 192 respectively. This is also known as an analog loop back path 199 from the transmitter to the transceiver." In paragraph [0021], Kakizawa further teaches "positive and negative receiver pins 210 and 212 are coupled to the positive and negative transmitter pins 110 and 112 (referring to figure 1), respectively, via the transistors 290 and 292. As discussed above, coupling the receiver pins 210 and 212 to the transmitter pins 110 and 112 provides an analog loop back path 299 to enable the

semiconductor device to perform self-tests on the input/output interface of the semiconductor device.” Accordingly, although different reference numbers are used, Kakizawa describes the same path in both instances. The attached figure combines Figures 1 and 2 of Kakizawa to show this common path.

In addition, Kakizawa further does not suggest a plurality of internal test signal paths between an input pad and an output pad as recited in pending claims 1, 13, and 14. Rather, for additional varieties of testing, Kakizawa discloses using external circuitry as stated in paragraph [0027]: “The trace lines 340 provide an *external* data loop back path from the transmitter 320 to the receiver 310 to enable the transmitter 320 and the receiver 310 to perform self-tests, which may include various leakage tests.” For this reason, a person skilled in the art following Kakizawa’s teaching would not provide for internal signal paths for testing but would instead provide for additional *external* signal paths as it is taught by Kakizawa.

Please consider these sections of the disclosure of Kakizawa and how they relate to the arguments that have been previously presented regarding the feature of a plurality of switching transistors providing for a plurality of internal test signal paths between an input pad and an output pad.

